

## Chapter

## 6

## Software Specifications

*Get to know more about the S6Fm series Notebook with a detailed look at the software specifications.*

The information contained in the chapter can be quite useful when you are troubleshooting the system's hardware. Each item has its individual usage for you to understand the software side of the notebook's architecture.

## 1. Introduction

This BIOS specification describes the major features of key components and system BIOS, the usage of general purpose input/output (GPIO) pins of south bridge (SB) and embedded controller (EC), the hardware IRQ routing and resource allocation, setup menu, system power management mechanism, system security policy, and so on.

The system BIOS is designed to comply with all industry standards, specifications, and design guides of PC/AT system including:

- PC 2001 System Design Guide, Version 1.0
- Advanced Configuration and Power Interface (ACPI) Specification, Revision 1.0b & 2.0
- Simple Boot Flag Specification, Revision 2.0
- PCI BIOS Specification, Revision 2.0
- Plug and Play BIOS Specification, Version 1.0A
- Extended System Configuration Data (ESCD) Specification
- System Management BIOS (SMBIOS, i.e. DMI) Reference Specification, Version 2.3
- System Management Bus BIOS Interface Specification, Revision 1.0
- BIOS Boot Specification
- Multiprocessor Specification, Revision 1.4
- Universal Serial Bus Specification, Revision 1.1 & 2.0
- Universal Host Controller Design Guide
- Universal Serial Bus PC Legacy Compatibility Specification
- Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0
- PCI Express Base Specification, Revision 1.0
- PCI Local Bus Specification, Revision 2.3
- PCI Bus Power Management Interface Specification

This specification is one of the porting guides of system BIOS for engineers and is for internal use only. Anyone who needs the information of system BIOS could also refer to it. Any question about this specification, please feedback to [Nicole\\_Pei@asus.com.tw](mailto:Nicole_Pei@asus.com.tw)

## 1. Hardware Overview

### 1.1. Key Components

The onboard key components and optional mini-PCI modules are listed at table 2-1 and 2-2.

Table 1-1 Key Component List

Item	Vendor	Part's Name	Features
CPU	Intel	Yonah Merom	Geyserville III Speed-Step Thermal Monitor 2
North Bridge	Intel	945-GM	Support 533,667Hz processor NEW: Support DDR & DDR2 SDRAM
South Bridge	Intel	ICH7-M	NEW: Support Azalia Interface. NEW: Support SATA interface. NEW: Support 6 PCI Express root ports.
VGA	Intel	945-GM	PCI Express graphic chip.
USB	Intel	ICH7-M	Support USB SPEC. 1.0, 1.1 & 2.0.
LAN	Realtek	RTL-8111B	Support 10/100/1000Mb/s.
IEEE1394	Ricoh	R5C832	
Azalia Audio codec	Realtek	ALC660 Ver.D	Support 7.1 audio channels.
Clock Gen.	ICS	ICS954310	Provide clock to system.
Thermal	ANALOG DEVICES	ADT7473	Control fan and thermal trip.
Azalia Modem codec	Motorola	ML3054	Function like as MC97 modem.
Embedded Controller	Mitsubishi	M38857	Keyboard, mouse, brightness and EC SCI control.

Table 1-2 Optional Component List

Item	Vendor	Part's Name	Revision
Wireless LAN	Intel	3945ABG\4965AGN	

### 1.2. Bus Number Allocation

The bus number allocation for PCI-to-PCI and PCI Express Graphic bridges are listed at table 2-3.

Table 1-3 Bus Number Allocation

Device	Bus#	Dev#	Fun#	Primary Bus#	Secondary Bus#	Subordinate Bus#	Onboard Devices On Secondary Bus
PCI-to-PCI Bridge	0	30	0	0	5	5	1394
PCI Express Root Port 0	0	28	0	0	1	1	LAN
PCI Express Root Port 1	0	28	1	0	2	2	Wireless LAN
PCI Express Root Port 2	0	28	2	0	3	4	New Card
I.G.D.* Bridge	0	2	0	0	0	0	PCI Express Graphic Controller

\*: I.G.D. – PCI Express Graphic

### 1.3. IRQ Routing of PCI Devices

The IRQ routing of onboard PCI chipsets and mini-PCI slot are shown at table 2-4.

Table 1-4 IRQ Routing of Onboard PCI Chipsets and mini-PCI Slot

Device	Vendor	IDSEL	Bus#	Dev#	Fun#	INTA	INTB	INTC	INTD
I.G.D. VGA	Intel	AD16	0	2	0	PIRQA			
Azalia Controller	Intel	*	0	27	0	PIRQF			
PCI Express Root port 0	Intel	*	0	28	0	PIRQA			
PCI Express Root port 1	Intel	*	0	28	1	PIRQB			
PCI Express Root port 2	Intel		0	28	2	PIRQC			
USB #0	Intel	*	0	29	0	PIRQH			
USB #1	Intel	*	0	29	1		PIRQD		
USB #2	Intel	*	0	29	2			PIRQC	
USB #3	Intel	*	0	29	3				PIRQG
EHCI	Intel	*	0	29	7	PIRQH			
IDE #0 (PATA)	Intel	*	0	31	1	PIRQC**			
1394	Ricoh	AD16	5	3	0	PIRQF			
SD Card	Ricoh	AD16	5	3	1		PIRQB		
MMC	Ricoh	AD16	5	3	2		PIRQE		
Memory Stick	Ricoh	AD16	5	3	3		PIRQE		
xD-Picture card	Ricoh	AD16	5	3	4		PIRQE		

\*: Chipset Internal Routing

\*\*: Chipset Internal Routing at NATIVE mode

IRQs Available for PIRQA~PIRQH on PIC-Enabled O.S. are:

3, 4, 5, 6, 7, 11

IRQs Available for PIRQA~PIRQH on APIC-Enabled O.S. are:

PIRQA – 16, PIRQB – 17, PIRQC – 18, PIRQD – 19

PIRQE – 20, PIRQF – 21, PIRQG – 22, PIRQH – 23

### 1.4. PCI Device IDs

The vendor/device and sub-system/sub-vendor IDs of onboard PCI devices are listed at table 2-5.

Table 1-5 Vendor/Device & Sub-System/Sub-Vendor IDs

Device	Vendor	Bus	Dev.	Fun.	Vendor ID	Device ID	Sub-Vendor ID	Sub-System ID
Host Bridge	Intel	0	0	0	8086	27A0	1043	12A7
VGA	Intel	0	2	0	8086	27A2	1043	1252
VGA#1	Intel	0	2	1	8086	27A6	1043	1252
LPC	Intel	0	31	0	8086	27B9	8086	27B9
SATA IDE	Intel	0	31	1	8086	27DF	1043	12A7
PCI EXPRESS Root Port	Intel	0	28	0	8086	27D0	n/a	n/a
USB0	Intel	0	29	0	8086	27C8	1043	12A7
USB1	Intel	0	29	1	8086	27C9	1043	12A7
USB2	Intel	0	29	2	8086	27CA	1043	12A7
USB3	Intel	0	29	3	8086	27CB	1043	12A7
EHCI	Intel	0	29	7	8086	27CC	1043	12A7
Azalia controller	Intel	0	27	0	8086	27D8	1043	1339

<b>LAN</b>	Realtek	1	0	0	10EC	8168	1043	11F5
<b>Wireless</b>	Intel	2	0	0	8086	4222	8086	1001
<b>IEEE 1394</b>	Ricoh	5	3	0	1180	0832	1043	12A7
<b>SD</b>	Ricoh	5	3	1	1180	0822	1043	12A7
<b>MMC</b>	Ricoh	5	3	2	1180	0843	1043	12A7
<b>Memory Stick</b>	Ricoh	5	3	3	1180	0592	1043	12A7
<b>xD-Picture card</b>	Ricoh	5	3	4	1180	0852	1043	12A7

## 1.5. Chipset Strapping

The strapping signals are used for static configuration. Table 2-6 and 2-7 show the strapping pins' driven states of SB and EC for the system.

Table 1-6 ICH7 Strapping Pin States

Pin Name	Usage	Strapping State	Function
GNT3#	Top-Block Swap Override	Low	The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the "top-block swap" mode (ICH7 inverts A16 for all cycles readable via the Top Swap bit (Chipset Config Registers: Offset 3414:bit 0)). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down
SPKR	No Reboot	High	The signal has a weak internal pull-down. If the signal sampled high, this indicates that the system is strapped to the "No Reboot" mode (ICH7 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config registers: Offset 3410:bit5)
INTVRMEN	Integrated VccSus1_5 VRM Enable / Disable	Low	Enable integrated VccSus1_5 VRM when sampled high
GPIO25	Reserved	Low	This signal has a weak internal pull-up. <b>NOTE:</b> This signal should not be pulled high.
GNT[5]#/GPIO17#, GNT4#/GPIO48	Boot BIOS Destination Selection	11b	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-ups. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h: bit 11:10) (GNT5# is MSB) 01-SPI 10-PCI 11-LPC
ACZ_SDOUT	XOR Chain Entrance / PCI Express Port Config bit1.	Internal pull low	Allow entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit 1 of PRC.PC (Chipset Config Registers :Offset 0224h). This signal has a weak internal pull-down.
ACZ_SYNC	PCI Express Port Config bit 1	Internal pull low	This signal has a weak internal pull-down. Set bit 0 of PRC.PC (Chipset Config Registers :Offset 0224h).

Table 1-7 M38857 Strapping Pin States

Pin Name	Usage	Strapping State	Function
P2.1	Enable/Disable Power Button Override feature	Low	Disable P5.4 Power button input function

## 1.6. Multiplex Pin Assignment and GPIO Pin Definition

The GPIO pin assignment of south bridge (SB) and embedded controller (EC) are shown at table 2-8 and 2-9. Some of multiplex GPIO pins should be initialized by system BIOS as general purpose input or output pins. The “#” symbol at the end of the signal name indicates that the active (or asserted) state occurs when the signal is at a low voltage level, i.e. low active.

Table 1-8 ICH7 GPIO Definition

GPIO Pin	I/O Type	Multiplex W/ Pin	Usage	Description
0*	I	BM_BUSY#	PM_BMBUSY#	Native Function
1	N/A	REQ5#	NOT USED	N/A
2	N/A	PIRQE#	NOT USED	N/A
3	N/A	PIRQF#	NOT USED	N/A
4	N/A	PIRQG#	NOT USED	N/A
5	N/A	PIRQH#	NOT USED	N/A
6	O	None	Back_OFF#	Turn on/off LCD's backlight
7	I	None	WIRELESS_SW#	Turn Off WIRELESS
8	I	None	EXTSMI#_3A	EC's SMI event
9	I	None	SATA_DET#	SATA_DET#
10	I	None	CHG_FULL_OC	Battery charge full indicator (HIGH – full, LOW – charging)
11	N/A	SMBALERT#	NOT USED	N/A
12	I	None	KB_SCI#	EC's SCI event
13	I	None	MEM_ID0	MEM_ID0
14	I	None	MEM_ID1	MEM_ID1
15	O	None	802_LED_EN#	Turn on/off WLAN LED
16*	O	DPRSLPVR	PM_DPRSLPVR	Native Function
17	N/A	GNT5#	NOT USED	N/A
18*	O	STP_PCI#	STP_PCI#	Native Function
19	I	SATA1GP	PANEL_ID1	PANEL_ID1
20*	O	STP_CPU#	STP_CPU#	Native Function
21	N/A	SATA0GP	NOT USED	N/A
22	N/A	REQ4#	NOT USED	N/A
23	N/A	LDRQ1#	NOT USED	N/A
24	I	None	MEM_667/533#	Tell from DDR2 533 and 667
25	O	None	CB_SD#	Resume/suspend 1394 controller
26	O	EL_RSVD	OP_SD#	Turn On/Off speaker.
27	N/A	EL_STATE0	WLAN_ON#	Turn On/Off Wireless
28	I	EL_STATE1	MEM_667/533#	MEM_667/533#
29	N/A	OC#5	NOT USED	N/A
30	N/A	OC#6	NOT USED	N/A
31	N/A	OC#7	NOT USED	N/A
32*	N/A	CLKRUN#	PM_CLKRUN#	Native Function
33	O	AZ_DOCK_EN#	BT_ON/OFF#	Turn On/Off Bluetooth
34	O	AZ_DOCK_RST#	FWH_WP#	Protect/Unprotect EEPROM(Default value: High)
35	N/A	SATACLKREQ#	NOT USED	N/A

36	O	SATA2GP	BT_LED_EN#	Enable BlueTooth LED
37	I	SATA3GP	PCB_ID0	1 <sup>st</sup> PCB ID pin
38	I	None	PCB_ID1	2 <sup>nd</sup> PCB ID pin
39	I	None	MEM_ID2	MEM_ID2
40**	N/A	N/A	N/A	N/A
41**	N/A	N/A	N/A	N/A
42**	N/A	N/A	N/A	N/A
43**	N/A	N/A	N/A	N/A
44**	N/A	N/A	N/A	N/A
45**	N/A	N/A	N/A	N/A
46**	N/A	N/A	N/A	N/A
47**	N/A	N/A	N/A	N/A
48	N/A	GNT4#	NOT USED	N/A
49*	O	CPUPWRGD	CPUPWRGD	Native Function

\*: Not implemented as GPIO but native function pin.

\*\*: Not implemented.

Table 1-9 M38857 GPIO Definition

Pin	I/O Type	Usage	Description
2.0	O	KBCRSM	Connected to power button for triggering power button press and release events.
2.1	N/A	NOT USED	
2.2	O	BAT_LEARN	This pin is used for battery learning (refresh). Set it low for charging a battery or batteries and high for discharging a battery or batteries.
2.3	O	MSK_LEARN	Clear status of INSTANT_FUN#
2.4	O	SET_PCIRSTNS#	Set PCI reset
2.5	O	CAP_LED#	CAP Lock Indicator.
2.6	O	NUM_LED#	Number Lock Indicator
2.7	O	SCR_LED#	Scroll Lock Indicator
4.0	O	KBC_EXTSMI	Any system management interrupt will be issued through this pin. It will notify the system that some events happened.
4.1	N/A	NOT USED	
4.2	N/A	NOT USED	
4.3	O	BT_ON/OFF#	Turn On/Off Bluetooth
4.4	O	KBCPURST_3Q	CPU reset signal from KBC
4.5	O	KBC_GA20	A20 is gated by this pin from KBC.
4.6	O	KBCSCI_3Q	SCI pin to notify system of runtime or wake up events from KBC.
4.7	I	PM_CLKRUN#	Standard PCI clock run protocol
5.0	I	BAT_LLOW#_OC	Battery Low event
5.1	N/A	NOT USED	
5.2	N/A	NOT USED	
5.3	N/A	NOT USED	
5.4	I	LID_KBC#	LID switch event
5.5	I	BAT_IN_OC#	Low level indicates that battery is existed.
5.6	O	FF_INT	HD Protection IC
5.7	O	ADJ_BL	Adjust LCD brightness
6.0	I	PP_TPM	PP_TPM
6.1	I	CPPE_#_DET	It indicates that New Card is plug-in
6.2	O	RST#_NEWCARD	Reset New Card about 0.5sec(Optional)
6.3	O	CPPE__EN	Give power to SB PCIE
6.4	I	ACIN_OC#	High level indicates that AC adapter is existed.
6.5	I	BAT_SAVING#	Read VID's voltage
6.6	N/A	NOT USED	
6.7	N/A	NOT USED	
7.6	I/O	SMD_BAT	Monitor/ Control battery.
7.7	I/O	SMC_BAT	Monitor/ Control battery.

## 1.7. System Management Bus Connections

The system has three independent system management bus (SMBus) interfaces on SB and EC chipsets, respectively. The devices connected to these 3 host interfaces are shown at table 2-10 and 2-11.

Table 1-10 SMBus Connections on South Bridge

Device	Address	Usage
1 <sup>st</sup> DIMM Module	1010000xb*	Read DRAM timing and configuration stored on "Serial Presence Detect" (SPD) device of a DIMM module for determining memory size and optimum timing.
Clock Generator	1101001xb	Disable unused clock source and enable spread spectrum.
Thermal Monitor	1001100xb	Set thermal trip and automatic fan on points; Provide current temperature

\*: Where x=1 – READ, x=0 – WRITE.

Table 1-11 SMBus Connections on Embedded Controller

Device	Address	Usage
Smart Battery	0001011xb	Access gas gauge for getting design/remaining capacity, charging/discharging state, etc.

## 1.8. Display Data Channels (DDC) and GMBus

The VGA controller supports display data channels (DDC) on LCD, CRT, and SDVO interfaces as well as SMBus on SDVO. Thus, the VGA BIOS and driver could determine the resolution and timing of a display device by reading its EDID data. The system BIOS doesn't have to provide callback function for reporting LCD type.

Table 1-12 DDC and GMBus Connections on VGA Controller

Device	Address	Usage
LCD Panel		Access EDID data for determining the resolution and timing of the display device
CRT Monitor		Ditto.

## 1.9. LED Indicators

The colors and states of system LED indicators are described at table below.

Table 1-13 Colors and States of LED Indicators

LED	State	Color	Indication
Power	Steady On	Blue	System power is supplied
Power	Flashing	Blue blinking	S3 (suspend to RAM) state
Battery-Charging	Steady On	Orange	Charge a battery or batteries
Battery Low Power	Flashing	Orange blinking	Battery capacity is below 10%
Hard Disk	Flashing	White	Access a hard drive
CAPS Lock	Steady On	White	CAPS Lock enable/ disable
WLAN	Steady On	Blue	Wlan on/off
Bluetooth	Steady On	White	Bluetooth on/off

## 1.10. General Purpose Events of South Bridge

The general-purpose inputs of the south bridge could trigger SCI, SMI, and/or wake-up events. These inputs come from LID switch, EC, USB, LAN, modem, and audio interfaces. Table 2-14 lists the general-purpose event (GPE) connections.



Table 1-14 GPE Connections on SB

Source	GPE#	ACPI Mode			Legacy Mode		
		SCI	SMI	Wake	SCI	SMI	Wake**
Thermal (THRM#)	0	V				V	
Battery Low (PIC)	20h	V				V	
EC's SCI Pin (P46)	22h	V				V	
EC's SMI Pin (P40)	1Eh		V			V	
LAN's PME*	0bh			V			
Ring Indication (RI#)	08h			V			
Modem CODEC	05h			V			
Audio CODEC	05h			V			
USB0	03h			V			
USB1	04h			V			
USB2	0Ch			V			
USB3	0Eh			V			
EHCI	0Dh			V			

\*: PME – Power Management Event

\*\*: Because the chipset doesn't support S1 state and the BIOS do not support S3 state for none ACPI O.S., either, it actually has no sleep state at legacy mode.

## 1.11. Events of Embedded Controller

The internal keys and general-purpose input pins are the SCI, SMI, and WKI event sources of the embedded controller (EC). The event sources of this system are shown at table below.

Table 1-15 SCI, SMI, and WKI Events of Embedded Controller

Source	Notification Code (Hex.)	Trigger Pin		Function
		ACPI Mode	Legacy Mode	
Fn+F1 (FHK1)	0Ah	SCI	SMI	Simulate a sleep button.
Fn+F2 (FHK2)	0Bh	SCI	SMI	Switch BT on/off.(canceled)
Fn+F3 (FHK3)	0Ch	SCI	X	Invoke E-mail
Fn+F4 (FHK4)	0Dh	SCI	X	Invoke Internet
Fn+F5 (FHK5)	0Eh	SCI	SMI	Decrease LCD brightness.
Fn+F6 (FHK6)	0Fh	SCI	SMI	Increase LCD brightness.
Fn+F7 (FHK7)	10h	SCI	SMI	Turn off LCD backlight.
Fn+F8 (FHK8)	11h	SCI	SMI	Toggle display devices.
Fn+F9 (FHK9)	12h	SCI	X	Switch Touchpad on/off
Fn+F10 (FHK10)	13h	SCI	SMI	Turn audio volume on/off.
Fn+F11 (FHK11)	14h	SCI	SMI	Decrease audio volume.
Fn+F12 (FHK12)	15h	SCI	SMI	Increase audio volume.
Fn+C (FHK14)	69h	SCI	X	Invoke Splendid (Color Enhance)
Fn+ Space (FHK19)	6Eh	SCI	X	Invoke Power4Gear
Fn+ T (FHK20)	6Fh	SCI	X	Invoke Power4Phone
M_MODE (P65)	35h	SCI	X	Invoke a designated application program.
Fn+ESC (FHK13)	68h	SMI	SMI	Break into debugger.
AC_IN (P64)	34h	SCI	SMI	Notify if the AC power is supplied or cut off.
BAT_IN# (P55)	2Fh	SCI	SMI	Notify if a battery is plugged in or removed
Any Key being pressed at suspend state	28h	WKI	WKI	Wake up a system from sleep state.

NOTE: The WKI (KBCRSM) pin is connected to power button switch. So, it looks like a power button is being pressed when typing any key of internal keyboard.

## 1.12. Clock

To reduce EMI, it should disable these clock source not being used according. In the system, the clock generator is the clock source for all chipsets and the memory controller provides the clock source for DRAM DIMM modules. The connections of these clock sources are shown at table 2-16 and 2-17.

Table 1-16 Clock Source on Memory Controller

Source Pin(s)	Connected to	Control Register
SM_CK[1:0] SM_CK[1:0]#	DIMM #0	MCHBAR* + 10Ch[1-0]
SM_CK[4:3] SM_CK[4:3]#	DIMM #1	MCHBAR + 18Ch[1-0]

\*: GMCH Register Range Base Address (Bus#0/Dev#0/Func#0/Reg#44h).

Table 1-17 Clock Source on Clock Generator

Source Pin(s)	Connected to	Control Register	Free Running
CPUCLKT1/CPUCLKC1	CLK_MCH_BCLK pin	BYTE1/BIT2	Y
CPUCLKT0/CPUCLKC0	CLK_CPU_BCLK pin	BYTE1/BIT1	N
SRCCLKT6/SRCCKLC6	CLK_PCIE_LAN pin	BYTE1/BIT3	
SRCCLKT5/SRCCKLC5	CLK_PCIE_MINICARD0 pin	BYTE0/BIT5	
SRCCLKT3/SRCCKLC3	CLK_MCH_3GPLL pin	BYTE0/BIT3	
SRCCLKT0/SRCCKLC0	CLK_TPMPCl pin	BYTE0/BIT0	
DOTT_96MHz/DOTC_96MHz	DREFCLKIN pin	BYTE1/BIT1	
USB_48MHz	SB USB CLK48 pin	BYTE1/BIT5	
PCICLK2	CLK_SIOPCl pin	BYTE2/BIT6	
PCICLK3	CLK_KBCPCl pin	BYTE2/BIT7	
PCICLK4	CLK_CBPCl pin	BYTE1/BIT7	
PCICLK5	CLK_TPMPCl pin	BYTE2/BIT3	
PCICLK_F0	CLK_ICHPCl	BYTE2/BIT4	

## 2. BIOS Function

The main features of the BIOS are shown at table 3-1. It's major change is not supporting APM function because all supported Operating Systems except DOS are ACPI-Enabled and the core chipset doesn't support S1 sleep (power on suspend) state. It, thus, has no suspend state available at DOS.

Table 2-1 Features of System BIOS

Item	Description
BIOS	AMI CORE8; 4Mbits Firmware Hub (FWH) EEPROM
CPU / Cache	Automatic frequency and cache size detection; Dynamic CPU speed control at Windows XP ("Windows Native Processor Performance Control"); Static CPU speed control during POST and at DOS.
DRAM	Sizing and timing detection by SPD.
HDD/CDROM	4-drive, Fast DMA, UDMA, fast PIO, block PIO, 32-bit IO, SMART disk, and INT 13 extensions support; automatic model typing, size detection, and parameters setting (drive geometry, transfer mode, block size, LBA); bootable CDROM; hot swapping.
FDD	N/A
Bootling	Quiet boot; quick boot; multi-boot from HDD, CDROM, LAN (PXE), and USB devices peripheral; boot sequence control at setup menu and pop-up boot selection menu.
Setup Menu	Press F2 to enter setup menu during POST. For details, please refer to setup menu section.
Boot Selection Menu	Press ESC to pop-up this menu to select a boot device for one time.
Display	Multiple I.G.D. controller support; LCD, CRT, and TV presence detection and toggle.
Keyboard	US/JP/EU internal keyboards and USB keyboard support.
Mouse	Internal touch pad, PS/2 mouse, and USB mouse Support.
Parallel port	N/A
Security	User & Supervisor password control for setup menu and boot; Hard disk locking and password-freezing control; USB, LAN, WLAN, MODEM, and Audio interfaces-disabling control.
PnP	Legacy ISA, PnP ISA, PCI and PCIExp devices auto-configuration; PnP ISA and PCI run-time BIOS services support.
APM	Not support.
ACPI	C0, C1, C2, C3 (or C4), S0, S3, S4, and S5 power management states; control method battery; proprietary on-screen display utility support.
SMBus	SMBus run-time BIOS services.
DDC	Display Data Channel is supported by built-in VGA BIOS.
SMBIOS (DMI)	System Management BIOS v.2.3 support. Windows DMI data update interface support.
M-Mode	Dynamic CPU speed control.
Flash	EzFlash during POST; DOS and Windows flash interface support.
Others	Daylight savings time; Fast A20; 32-bit BIOS services; graphic setup menu (English only).

### 2.1. Memory

The BIOS automatically detects the amount of memory in the system and configure the DRAM timing based on the SPD data of DIMM module(s) at beginning of POST (Power-On-Self-Test).

### 2.2. Display

In system BIOS, it adopts Intel VBIOS. The VGA BIOS callback function interface is also ready for VGA controller to select boot display device(s) and toggle them. The display device combinations of VGA

controller are shown at tables in this section. Additionally, the resolutions and timings of display devices are determined by their EDID data.

Table 2-2 Display Device Combinations for Intel's VGA

Display Device(s)	Primary	Secondary
CRT	Y	Y
LCD	Y	Y
TV	Y	Y
CRT + LCD	N	N
CRT + TV	N	N
LCD + TV	N	N

## 2.3. Enhanced IDE

The BIOS supports the LBA re-mapping method to translate the geometry of a hard disk drive and the INT 13 extension functions for removable devices and hard drives. On the system, it has two built-in IDE controllers: one is parallel ATA (PATA) interface and the other is serial ATA (SATA) interface that could be configured to run at legacy IDE mode or AHCI mode. Both controllers support only one channel, i.e. two controllers totally support two channels. The BIOS will configure these two IDE controllers based on the attached IDE drives and user's selection at setup menu. The configurations are shown at table below.

Table 2-3 PATA and SATA Configurations

Configuration Selection	Present Device(s)	Controller		Running Mode	
		PATA	SATA	PATA	SATA
Compatible	None or PATA only	Enabled	Disabled	Legacy	
Compatible	SATA only	Disabled	Enabled		Legacy
Compatible	SATA & PATA	Disabled	Enabled		Legacy

Additionally, the BIOS also supports the IDE hot swapping function for the drive on PATA controller if the booting hard disk drive is on SATA controller.

## 2.4. Legacy USB

In addition to USB keyboard and mouse, the BIOS also support USB 2.0 and 1.1 peripheral devices including flash, hard disk, and optical drives for Operating Systems having no USB driver. In DOS, it should load an ASUS's proprietary USB driver to support DVDROM/CDROM drives.

## 2.5. Plug and Play

The BIOS supports the PnP, PCI, and ACPI specifications for dynamically allocating system resources. The resource allocation of system board devices is listed at table below.

Table 2-4 System Resource Allocation

Device	Connect Type	Resources				
		I/O (Hex)	IRQ at PIC	IRQ at APIC	DMA	Memory (Hex)
DMA Controller	Static	00~0F, 81~8F				
PIC Controller	Static	20~21, A0~A1				

Local APIC	Dynamic					FEE00000~FEExxxx
IOAPIC	Dynamic					FEC00000~FECyyyy
System Timer	Static	40~43	0	0		
RTC	Static	70~75	8	8		
System Speaker	Static	61				
System Board	Static	80				E0000~FFFFF
NB Chipset (System Board)	Static					E0000000~ EFFFFFFF, FED14000~ FED17FFF, FED18000~ FED18FFF, FED19000~ FED19FFF
SB Chipset (System Board)	Static	400~41F, 480~4BF, 800~87F				FED1C000~ FED1FFFF
Embedded Controller	Static	60, 62, 64, 66	1	1		
Math Coprocessor	Static	F0~FF	13	13		
Touch Pad / PS/2 Mouse	Static		12	12		
Video Controller	Static	3B0~3BB, 3C0~3DF	11			A0000~BFFFF, C0000~CFFFF
Serial Port	(NO)					
Fast IR / IrDA	(NO)					
ECP, Parallel port	(NO)					
FDC	(NO)					
PATA IDE Controller (Compatible Mode)		DISABLED				
SATA IDE Controller (Compatible Mode)	Static	170~177, 376, 1F0~1F7, 3F6	14, 15	14, 15		
PATA IDE Controller (Enhanced Mode)	Static	1F0~1F7, 3F6	14	14		
SATA IDE Controller (Enhanced Mode)	Dynamic					
1394 Controller	Dynamic					
Audio Controller	Dynamic					
Modem Controller	Dynamic					
USB Host Controller	Dynamic					
LAN Controller	Dynamic					
WLAN Controller	Dynamic					

Note: 1. The dynamic resource of devices will be changed if users change the settings.  
2. The system has no super I/O.

## 2.6. Power Management

The BIOS supports C0, C1, C2, C3 (or C4), S0, S3, S4, and S5 power management states for ACPI-Enabled Operating Systems. In DOS, it has no power management because the SB chipset

doesn't support S1 sleep state. It doesn't support Advanced Power Management (APM), either. Figure 1 shows the global system power states and transitions.

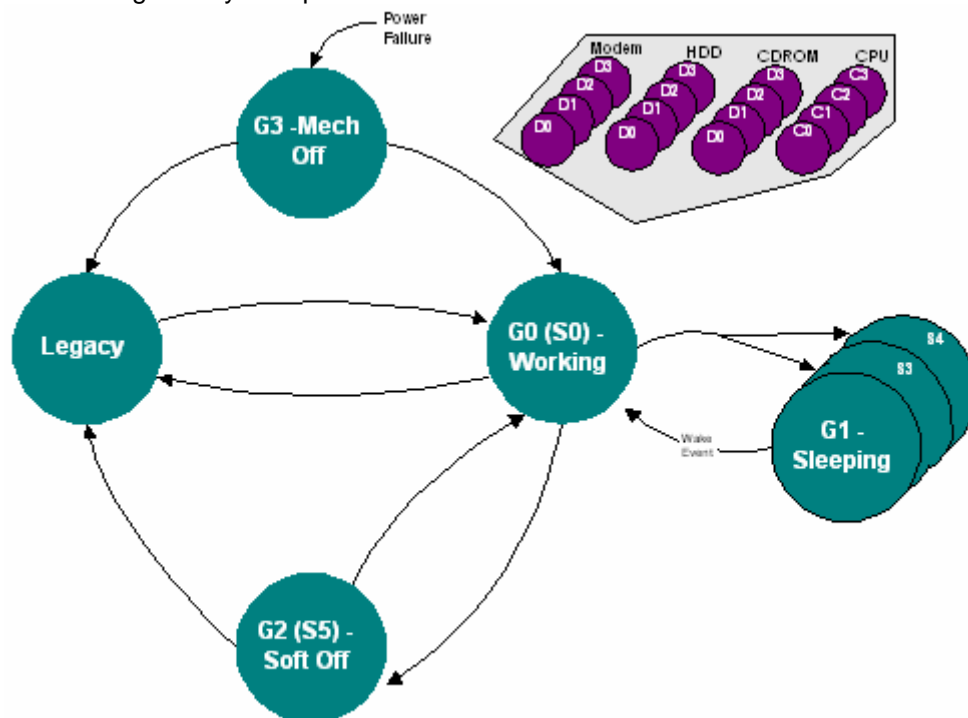


Figure 1 Global System Power States and Transitions

## 2.6.1. C States

To enhance system performance and save battery life, the BIOS uses the `_CST` control method to dynamically report the supported "C States" when powered by AC or by DC.

- Powered By AC: C2.
- Powered By DC: C2, C4

In `_CST` control method, it reports "level 4" I/O port at C3 state package buffer to force system entering C4 state when an O.S. puts CPU to C3 state because C4 state is not a standard "C" state of ACPI specification and not implemented by current Windows O.S. The C0 and C1 states are supported on all power sources. Any IRQ, SMI#, SCI, bus master, or FERR# event will bring the system to C0 state from C1, C2, C3, or C4.

For those O.S. such as Windows Me doesn't recognize `_CST` control method, the BIOS always reports the system supports C2 and C3 at "Fixed ACPI" (FACP) description table. The worst-case hardware latency times of C2 and C3 are 10 and 100 microseconds, respectively.

## 2.6.2. Sleep States

1. **S0 state:** The CPU and all devices are working.
2. **S3 state:** The CPU and PCI busses are powered off. All PCI devices must either be powered-off or isolated and the embedded controller is put into suspend state. However, the system memory and graphic frame buffer are powered and refreshed by the memory controller and the graphics controller, respectively. The system provides a 32kHz clock (SUSCLK) in this suspend mode to support refresh of these memory subsystems. Only enabled "resume event" such as internal keyboard, RTC alarm, power button, LAN, WLAN, Modem, USB device(s) can bring the platform out of this sleep state.
3. **S4 state:** The context of entire system devices and memory are saved to disk. All components are powered-off and all clocks are stopped. Any enabled "resume event" such as power button, RTC, and/or LAN can bring the platform out of the S4 state.
4. **S5 state:** Same as S4 except not saving system context.

Table 2-5 Wake Up Events

Resume Event	S3	S4	S5	Screen
RTC Alarm (IRQ 8)	Y	Y	Y	OFF
Power Button	Y	Y	Y	ON
LID Switch	Y			ON
Modem RI#	Y			OFF
PCI PME# (LAN)	Y	Y	Y	OFF
AZALIA# (Modem CODEC)	Y			OFF
USB	Y			ON
Any Key*	Y			ON

\*: The EC's "Any Key" wake-up event pin is connected to the power button switch.

## 2.7. CPU Speed Control

To fulfill the Geyserville III technology of Intel's Pentium-M CPU, the BIOS implements the ACPI control methods including \_PDC, \_PCT, \_PSS, and \_PPC for supporting "Windows Native Processor Performance Control" to dynamically change CPU speed based on system loading and power scheme selected in Windows XP.

- **\_PDC:** Called by native processor performance driver to pass it's capabilities to BIOS; The BIOS saves the capability flag for other control methods. This flag indicates if a native performance processor driver is loaded.
- **\_PCT:** If native driver is loaded, the processor native interface is used for the Performance Control Object by declaring the CPU's performance control and status registers as functional fixed hardware objects. Otherwise, the SMI interface is used for the Performance Control Object by declaring the ACPI command (0x82) and status (0x83) ports as performance control and status ports.
- **\_PSS:** If native driver is loaded, reports the control and status values based on CPU's performance control and status registers. Otherwise, these values are reported based on ACPI command and status ports.
- **\_PCT:** Report "0" as the highest state to allow all states to be used when running on both AC adapter and battery (DC).

The BIOS also supports "Enhanced Intel SpeedStep Technology System Management Mode Interface" for Intel's SpeedStep Applet in Windows. The O.S. and Intel's SpeedStep Applet program will issue software SMI to get BIOS support. The default SMI port is 0B2h at Intel's Applet program. Here are functions on this SMI interface:

- **DISABLE:** SMI Port = OS Command value located in ACPI FADT table offset 55.  
Called by the O.S. supporting native processor performance control. The CPU speed transition should be controlled by the O.S. The BIOS only responds to get status and reports to the applet.
- **INITIALIZE:** SMI Port = 81h. Detect and identify operating states of onboard CPU.
- **CONTROL:** SMI Port = 82h, EAX = 47534982h, EBX = 0.  
Enable or disable SMI applet interface.
- **GET STATUS:** SMI Port = 82h, EAX = 47534982h, EBX = 1.  
Reports to the applet software the current CPU state, the maximum number of states supported, the current available number of states, the SpeedStep capability of the CPU, the setup mode, the AC status, the revision of this SMI interface, and the current state of CPU throttling.
- **SET STATE:** SMI Port = 82h, EAX = 47534982h, EBX = 2.  
Initiate a transition to the requested state.
- **SET SETUP:** SMI Port = 82h, EAX = 47534982h, EBX = 3.  
Save changes of operating mode to the CMOS register location of the setup menu item for Intel's Applet control.
- **GET INFO:** SMI Port = 82h, EAX = 47534982h, EBX = 4.  
Reports to the applet software the highest and lowest performance states as well as the duty cycle of throttling.
- **GET STATES:** SMI Port = 82h, EAX = 47534982h, EBX = 5.  
Reports the frequency of all supported states.



For details, please refer to the Intel's orange document "RS – Geyserville Technology BIOS Porting Guide".

## 2.8. Thermal Management

The thermal management is able to divide two parts. One is active cooling control (FAN) and the other is passive cooling control (CPU throttle). If the CPU temperature is over passive temperature, OS will start passive cooling.

There is only one fan in S6FmM. Each fan is controlled by ADT7473. It uses automatic & manual fan control method. The fan start temperature is 45 degrees centigrade and fan stop temperature is 40 degrees centigrade. The following parameters are set for ADT7473 auto fan control in order to reduce acoustics.

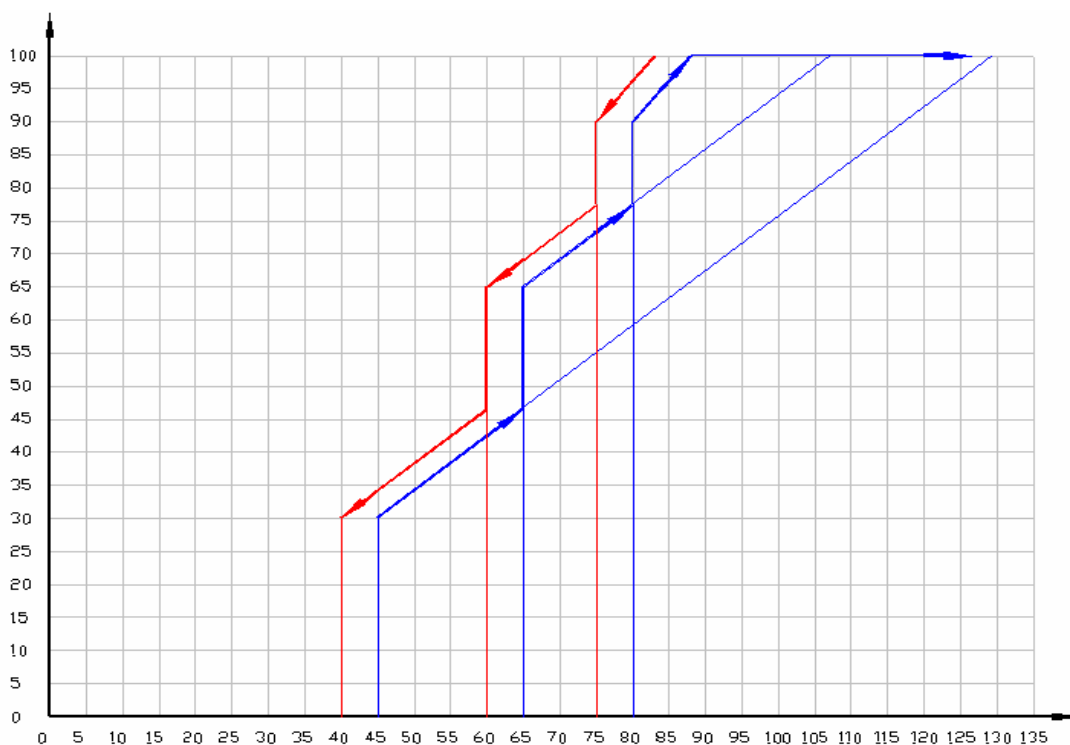
*FAN ON temperature is 45 degrees centigrade.*

*FAN OFF temperature is 40 degrees centigrade.*

*FAN full on temperature is 88 degrees centigrade.*

*FAN won't run at full speed when below 83 degrees centigrade.*

The figure below shows the fan PWM voltage versus temperature change.



### CPU Temperature Control

Low segment:

Tmin=45 \ Range=80 \ DC(min=30% /max=100%) \ Thyst=5

Middle Segment

Tmin=65 \ Range=80 \ DC(min=65% /max=100%) \ Thyst=5

High Segment

Tmin=80 \ Range=53.33 \ DC(min=90% /max=100%) \ Thyst=5

CPU Tj > 105 °C -> CPU Throttling

CPU Tj > 115 °C -> System Shutdown

Effective  
Trange

TDmax

TDmin

Trange

Tmax

Tmin

STEP1(L)	84.46	100.00	30.00	80.00	129.46	45.00
STEP2(M)	42.23	100.00	65.00 6-16	80.00	107.23	65.00
STEP3(H)	8.04	100.00	90.00	53.33	88.04	80.00



## 2.9. Brightness Control of LCD

To maintain a given user-perceive backlight brightness in the presence of an ever-changing ambient environment, the BIOS initializes embedded controller (EC) to automatically detect ambient light illumination via an ambient light sensor (ALS) and dynamically adjust the LCD's backlight. Additionally, it could save more system power for extending battery life.

During POST, the BIOS must load a patch binary code to EC RAM bank 8~14 and jump to its initialization routine. As well, the BIOS should configure it based on settings at last boot. In the patch code of the EC for ALS, it supports 8 brightness control scenarios (0~7) and 16 illumination levels (0~15). In addition, the brightness control range is divided into 16 levels. At scenario "0", the LCD's brightness level could vary in full brightness range (level 0~15). But it can only change in top 9 brightness levels (7~15) if scenario "7" is selected. Table 3-10 shows the brightness level versus illumination level at all scenarios. Please refer to the "Auto Brightness Control EC BIOS Software Specification" for details.

Together with ATK driver and application program, it could dynamically change the scenarios when pressing combination function key Fn+F5 or Fn+F6. It could also disable the automatic brightness control function to manually change the brightness when pressing Fn+F5 or Fn+F6. The detail of BIOS control method for supporting ALS is documented in "ASUS ACPI Application Program Specification".

Table 2-6 LCD Brightness Level V.S. Illumination Level at Different Brightness Control Scenario

Brightness Level Illumination Level	Brightness Control Scenario							
	0	1	2	3	4	5	6	7
0	0	1	2	3	4	5	6	7
1	1	2	3	4	5	6	7	8
2	2	3	4	5	6	7	8	9
3	3	4	5	6	7	8	9	10
4	4	5	6	7	8	9	10	11
5	5	6	7	8	9	10	11	12
6	6	7	8	9	10	11	12	13
7	7	8	9	10	11	12	13	14
8	8	9	10	11	12	13	14	15
9	9	10	11	12	13	14	15	15
10	10	11	12	13	14	15	15	15
11	11	12	13	14	15	15	15	15
12	12	13	14	15	15	15	15	15
13	13	14	15	15	15	15	15	15
14	14	15	15	15	15	15	15	15
15	15	15	15	15	15	15	15	15



Maximum brightness level index



Initial-working light sensor level

## 2.10. Embedded Controller

As well as keyboard controller, the embedded controller also includes the smart battery host controller and ACPI embedded controller (EC).

### 2.10.1. Functional Events

To easily adjust some system hardware settings such as flat panel backlight, audio volume, display device(s) or quickly bring up some predefined applications, the system implements the combination hot keys and buttons. When pressing those hot keys or buttons, the EC triggers SCI or SMI events depending on if ACPI mode is enabled or not. Additionally, the EC also triggers SCI or SMI event when plugging-in or removing an AC power adapter, a battery, or an IDE device at swapping bay. For the event codes and types, please refer to the section entitled "Events of Embedded Controller".

For SMI events, the EC's SMI handler of BIOS at SMM mode will query the SMI notification code of the EC event being triggered and dispatch its corresponding handler to toggle display devices, adjust LCD brightness, adjust audio volume, or change device in/out state and trigger polarity accordingly. For SCI events, the EC driver will query the notification code, say 2Ah, and call the corresponding \_Q control method, say \_Q2A, to handle the event. In turn, the \_Q control method notify ASUS's proprietary ATK driver to show On-Screen-Display (OSD) icons and do actions accordingly. Please refer to the ATK driver specification for the notification values of those events.

### 2.10.2. Wake-Up Event

The EC will be put into suspend state and powered when a system enters S3 state. It will pulse its wake-up pin when any key of the internal keyboard is pressed. Because the wake-up pin is connected to the power button switch, it, thus, seems to press the power button to wake the system.

### 2.10.3. Battery System

The battery system includes a charger and two smart batteries. Both charger and batteries are connected to the SMBus host interface of EC. A general-purpose pin is used to select one of two batteries to be connected to the SMBus interface at a time. The working mechanism of the battery system is as follows:

- The charger will stop charge the battery when the following condition is detected.
  - The temperature of the system is too high.
  - The battery voltage is too high.
- Battery Life is around ?? Hours.
 

Note that the battery life depends on different configuration running. (E.g. the battery life is shorter with CDROM running, the battery life is longer with document keyin only; battery life is short while power management is disabled, battery life is longer while power management is enabled.)
- Battery reading methodology is through power meter applet of control panel in Windows. The BIOS passes battery information to ACPI-enabled O.S. via control methods \_BIF and \_BST.
- When the battery capacity remains 10%\*, the charger will generate a battery warning SMI at none ACPI-enabled O.S. environment or a SCI at ACPI-enabled O.S. environment.
- When AC power is supplied, the battery system will do the following action:
  - The charger will charge the Battery.
  - The Battery Charging Indicator will turn on if the battery is in charging mode.
  - The "Battery Low" warning condition will be removed.
- When AC or battery power is supplied or removed, the EC will trigger events and the EC driver will call the \_Q control methods for AC and battery to handle these power events and notify O.S. to re-emulate the state and information of the battery system.

## 2.11. Security

To protect storage data and system, the BIOS implements several security mechanisms including setup menu protection, booting prevention, hard disk lock, I/O peripheral interface disable, and optional TPM module function.

### 2.11.1. Setup Menu and Booting Security

There are a supervisor and a user password for entering setup menu and booting a system. It could select to check these passwords only when entering setup menu. Please refer to "Security Menu" section for detail.

### 2.11.2. I/O Interface Security

The supervisor of a system could disable the modem, LAN, wireless LAN, USB, 1394, and optical drive devices at setup menu and limit user's access right to re-enable them.

### 2.11.3. Hard Disk Drive Protection

A user could set a password on a hard disk drive to lock it. At same time, a back door master password is also set on the drive. The hard disk will be locked when it's being hard reset. During POST, the BIOS will ask a user to input a password to unlock the drive. This password could be the user or master hard disk password. If the master password is input, the hard disk lock function will be disabled forever unless being re-locked again. Additionally, the user and master passwords are frozen after the drive is unlocked to prevent them from being changed by any application program. This input master password would be different everyday.

## 2.12. Crisis Recovery

A proprietary debug card is used for doing crisis recovery. The steps are:

1. Prepare one ISA EPROM with correct bios image.
2. Insert the ISA EPROM into a debug card
3. Select SW1:ON and SW3:OFF on debug card
4. Plug the debug card into a system.
5. Turn on the system.
6. The BIOS will execute normal POST and turn on screen before automatically recovering the system BIOS.
7. The BIOS will shutdown the system after finishing recovery.
8. Take out the debug card and turn on system power to boot from system BIOS.

## 2.13. Supported Utility

The BIOS supports 3 flash utilities that are running during POST, at DOS, or at Windows. In addition, it also supports a DOS and a Windows SMBIOS (DMI) utility for changing data of type 1, 2, and 3.

### 2.13.1. Extended 32 Bits Application Interface

It provides the interface to access hardware configuration for windows application.

The application tries to search the signature 'EXTF' from F000:0000h. Then, check the version of the structure of EXTF. If the version is greater than 00h, it represents supporting EXTF32 function.

As the result, the application could try to call the entry of EXTF32 interface at the offset 0Ah.

The functions provided by the EXTF32 interface are listed below.

**AH=80h,**

Reserved.

**AH=70h,**

For OEM implementation.

**CL=00h, Disable Resume Timer.**

Bios should disable any setting to avoid RTC wake up.

- (a). Clear IRQF, PF, AF, UF in CMOS 0Ch
- (b). Clear AIE in CMOS 0Bh.
- (c). Clear RTC\_EN in PMIO registers.

**CL=01h,****Get Resume Timer.**

Bios should return the resume timer settings to the application.

return :

CH = Second Alarm. (CMOS 01h)

DL = Minute Alarm. (CMOS 03h)

DH = Hour Alarm. (CMOS 05h)

SI = high byte : Month(CMOS 08h, no month alarm)

low byte : Date Alarm(chipset dependent)

DI = high byte : Century(BIOS dependent)

low byte : Year(CMOS 09h, no year alarm)

**CL =02h,****Set Resume Timer.**

Bios should set the resume timer for the application.

input :

CH = Second Alarm.

DL = Minute Alarm.

DH = Hour Alarm.

SI = high byte : Month

low byte : Date Alarm

DI = high byte : Century

low byte : Year

### 3. Setup Menu

S6FmM system BIOS allows users to change some system hardware/function settings during POST (power on self test) stage, users may hit F2 key to enter SETUP mode in POST, the setup feature is categorized into 6 menus described in next few sections

#### 3.1. Main Menu

Main menu describes system overall information with some user changeable setting, it contains below items:

BIOS SETUP UTILITY	
Main	Advanced Security Power Boot Exit
<div> System Overview </div> <hr/> <div> System Firmware  System BIOS Version : S6FmAS.202  VGA BIOS Version : 1270.I06802.003   Processor  Type : Intel(R) Core(TM)2 CPU L7200 @ 1.33GHz  Speed : 1334MHz   System Memory  Size : 1016MB   System Time [22:34:32]  System Date [Wed 01/10/2007] </div>	
<div> Use [ENTER], [TAB] or [SHIFT-TAB] to select a field.   Use [+] or [-] to configure system Time. </div>	
<div> ↔ Select Screen  ↑↓ Select Item  +- Change Field  Tab Select Field  F1 General Help  F9 Load Defaults  F10 Save and Exit  ESC Exit </div>	
v02.59 (C) Copyright 1985-2005, American Megatrends, Inc.	

1. Version: [xxxx.xxx] ← Current version for the system bios
2. Type [String]: What kind for CPU
3. Speed: The BIOS auto detect CPU speed, It's only show, so user don't modify
4. System Time: [hh/mm/ss] ← Current time
5. System Date [mm/dd/yy] ← Current date

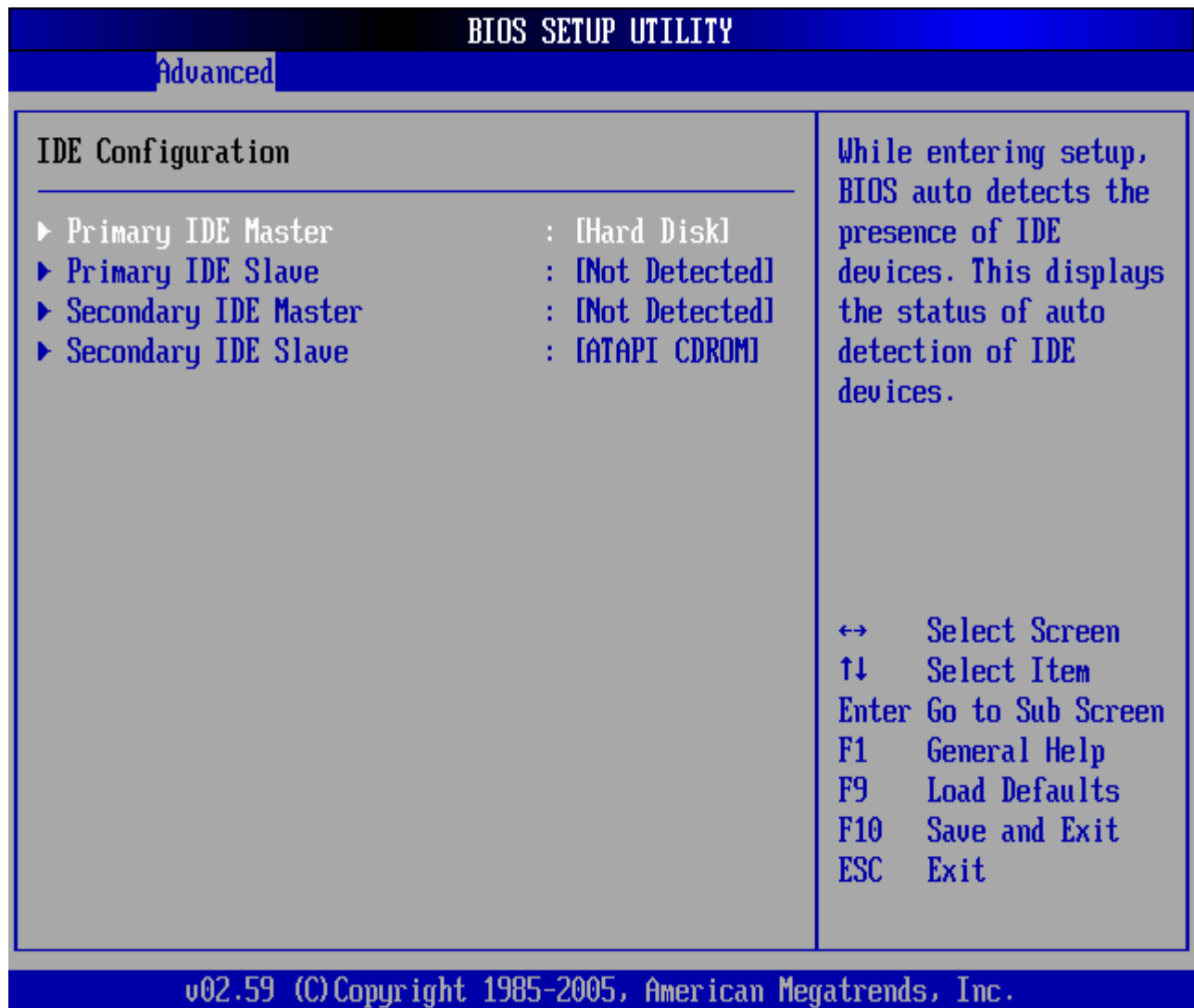
### 3.2. Advanced Menu

In advanced menu the users may configure I/O device resource such as I/O base, interrupt vector or DMA (Direct Memory Access) channel, some auxiliary settings may be changed as well. Detailed I/O device setting are described below:



1. IDE configuration: See 4.2.1
2. Internal pointing device: [Enable] ← Touch Pad enable/disable you can choice
3. Internal Numeric Pad Lock [Enable] ← Num LK (Number Lock) enable/disable
4. Play POST Sound [Yes] ← Enable/Disable Wave sound playing during Logo POST
5. Speaker Volume : [4] ← Adjust Volume from 0~8

### 3.2.1. IDE Configuration



## PRIMARY/SECONDARY MASTER/SLAVE IDE

BIOS SETUP UTILITY	
Advanced	
<b>Primary IDE Master</b>	
Device	:Hard Disk
Vendor	:ST9160821AS
Size	:160.0GB
LBA Mode	:Supported
Block Mode	:16Sectors
PIO Mode	:4
Async DMA	:MultiWord DMA-2
Ultra DMA	:Ultra DMA-6
S.M.A.R.T.	:Supported
LBA/Large Mode	[Auto]
Block (Multi-Sector Transfer)	[Auto]
PIO Mode	[Auto]
DMA Mode	[Auto]
S.M.A.R.T.	[Auto]
32Bit Data Transfer	[Enabled]
Disabled: Disables LBA Mode. Auto: Enables LBA Mode if the device supports it and the device is not already formatted with LBA Mode disabled.	
↔ Select Screen ↑↓ Select Item +- Change Option F1 General Help F9 Load Defaults F10 Save and Exit ESC Exit	
v02.59 (C) Copyright 1985-2005, American Megatrends, Inc.	

At system boot, the Intel Ultra ATA Storage Driver configures each ATA/ATAPI device to transfer data at particular transfer modes. These transfer modes are defined by ATA standards, and are either Programmed I/O (PIO) or Direct Memory Access (DMA or UltraDMA) type transfers. The Intel Ultra ATA Storage Driver usually configures devices for their fastest capable transfer modes; however, there may be times when a different (perhaps slower) transfer mode is appropriate for a particular device or system configuration.

For hard disk and CD-ROM drives BIOS detect them automatically. The users may enter the selected (highlighted) item to get more detailed information, which contains 3 selectable setting:

**[Auto]:** BIOS default setting.

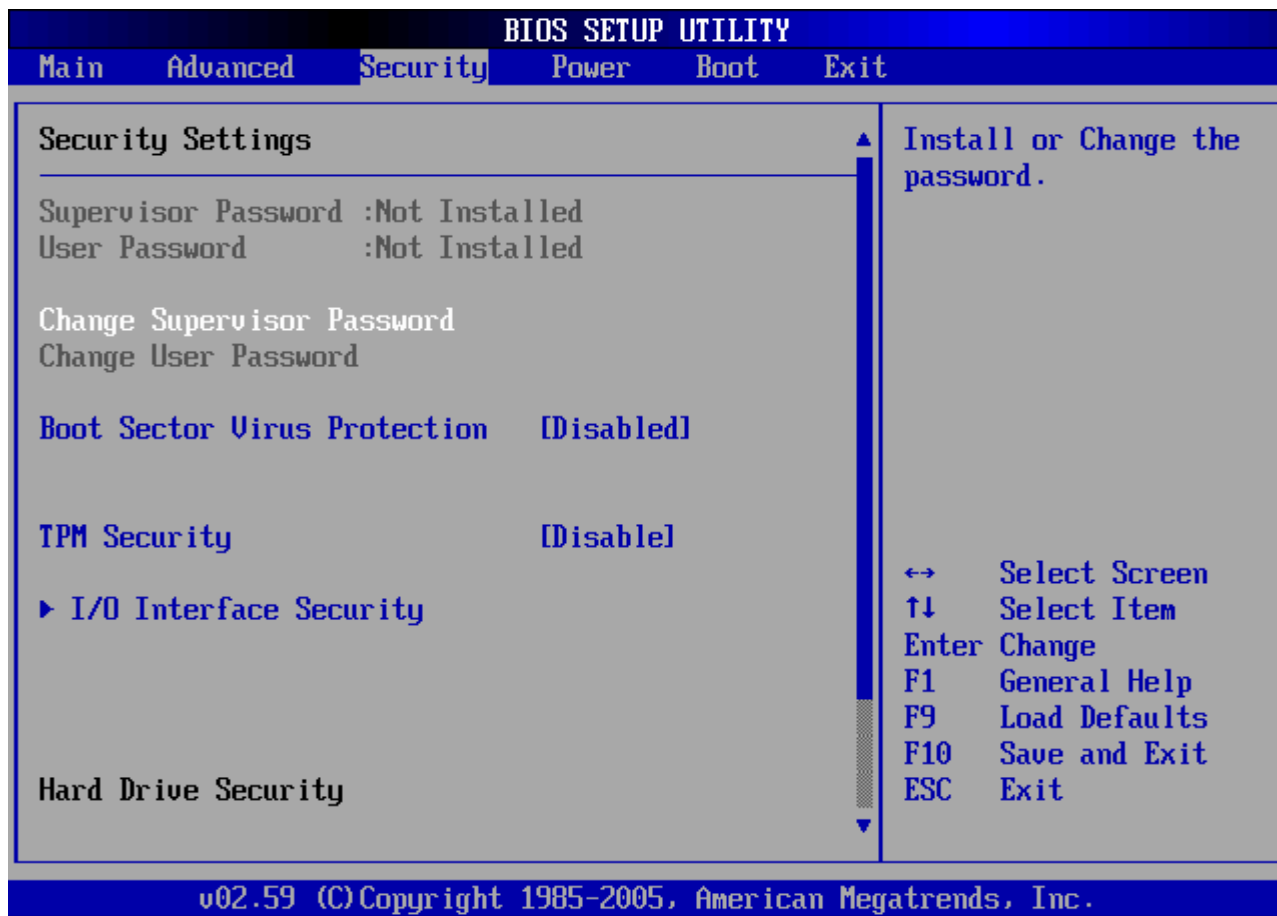
**[User Type HDD]:** Users may configure the disk geometry by changing below item:

- Translation Methods
- Cylinders
- Head
- Sector
- Multi-Sector Transfer
- Smart Monitoring
- PIO Mode
- Ultra DMA Mode

**[None]:** Hide the drive.



### 3.3. Security Menu



BIOS supports two levels of password for security protection:

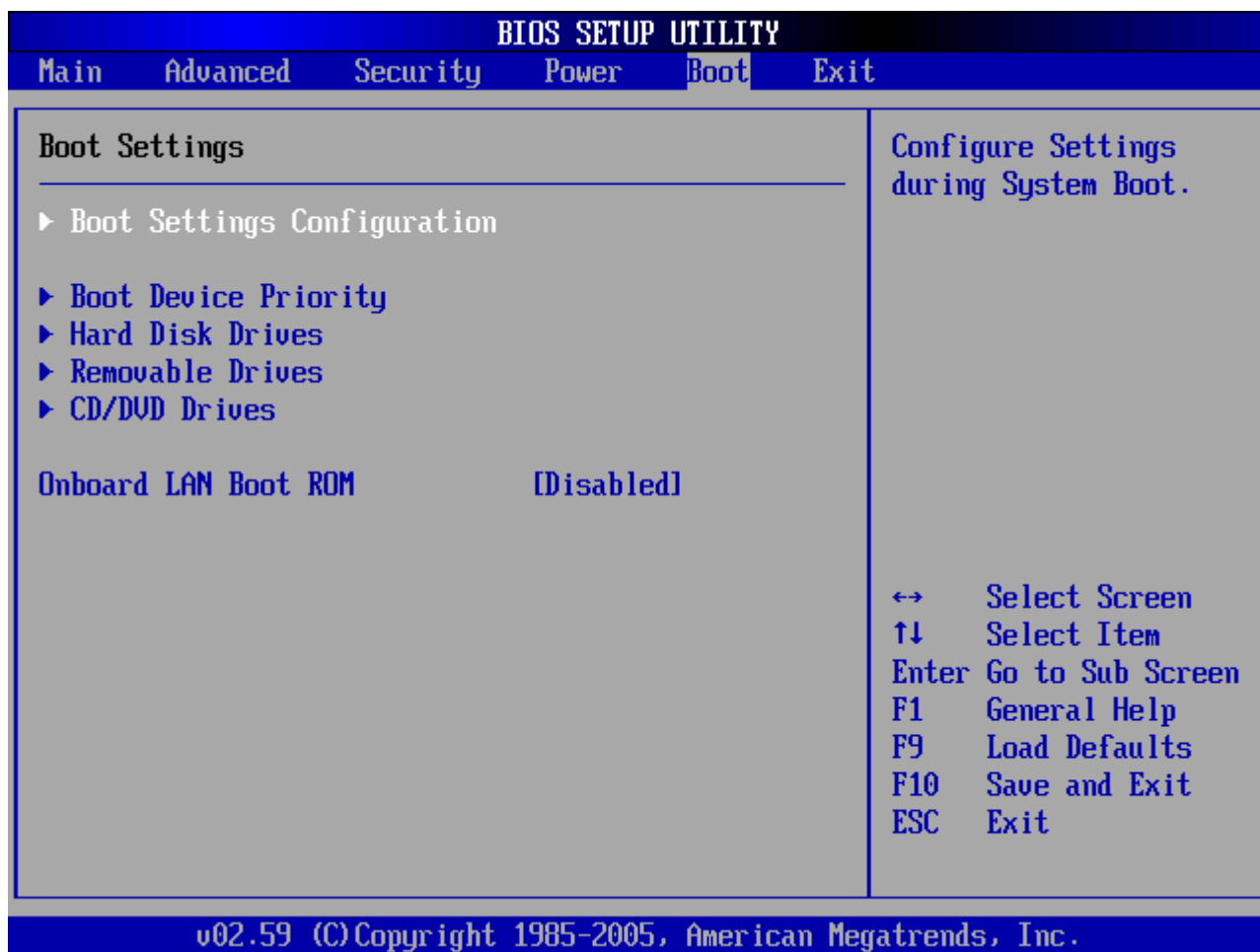
1. **Supervisor password:**  
 Users may set, change or erase system password, the password data is saved in non-volatile device (CMOS), system password check is done during POST (Power On Self Test). The BIOS will prompt a dialog message to ask user for password check when:  
 The system has password stored, and  
 "Password on boot" setting in BIOS SETUP is enabled.  
 If password verification fails for 3 times, the system BIOS will halt the machine to inhibit users from operating.
2. **User Password**  
 If other has modified your setting of BIOS, you can setting the function [Enable],  
 And type in your password and confirm, don't modify BIOS setting if no password.
3. **Hard disk password:**  
 Users may set, change or erase hard disk password, the password data is stored in the drive itself, the BIOS prompts a dialog message for hard disk password verification whenever it finds the hard disk locked in POST.  
 If hard disk password verification fails for 3 times, the system BIOS will halt the machine to inhibit users from operating.
4. **TPM Security:** Enable and disable TPM function.

### 3.4. Power Menu



- 1 LCD Power Saving:** LCD exhausts the most part of power while the system is operating. S6FmM notebook system BIOS support auto backlight saving mode. When the system BIOS detects AC adapter removal, the LCD brightness is tuned down to 80% of its original setting, and back to normal when AC adapter is back inserted.
- 2 Wake On Lan From System off :** Allow user to wake up system from S5(only supported under AC mode) via Magic Package (MAC address)
- 3 Battery refresh:** After long time incomplete charge/discharge cycles, the battery meter becomes less and less accurate (the total power capacity is not significantly affected, however). Battery gauge needs to “learn”, this item helps users to recalibrate the battery gauge. In the learning process, users need to follow system BIOS instruction to I  
Insert/remove the AC adapter so that a complete reset and learning cycle may start.

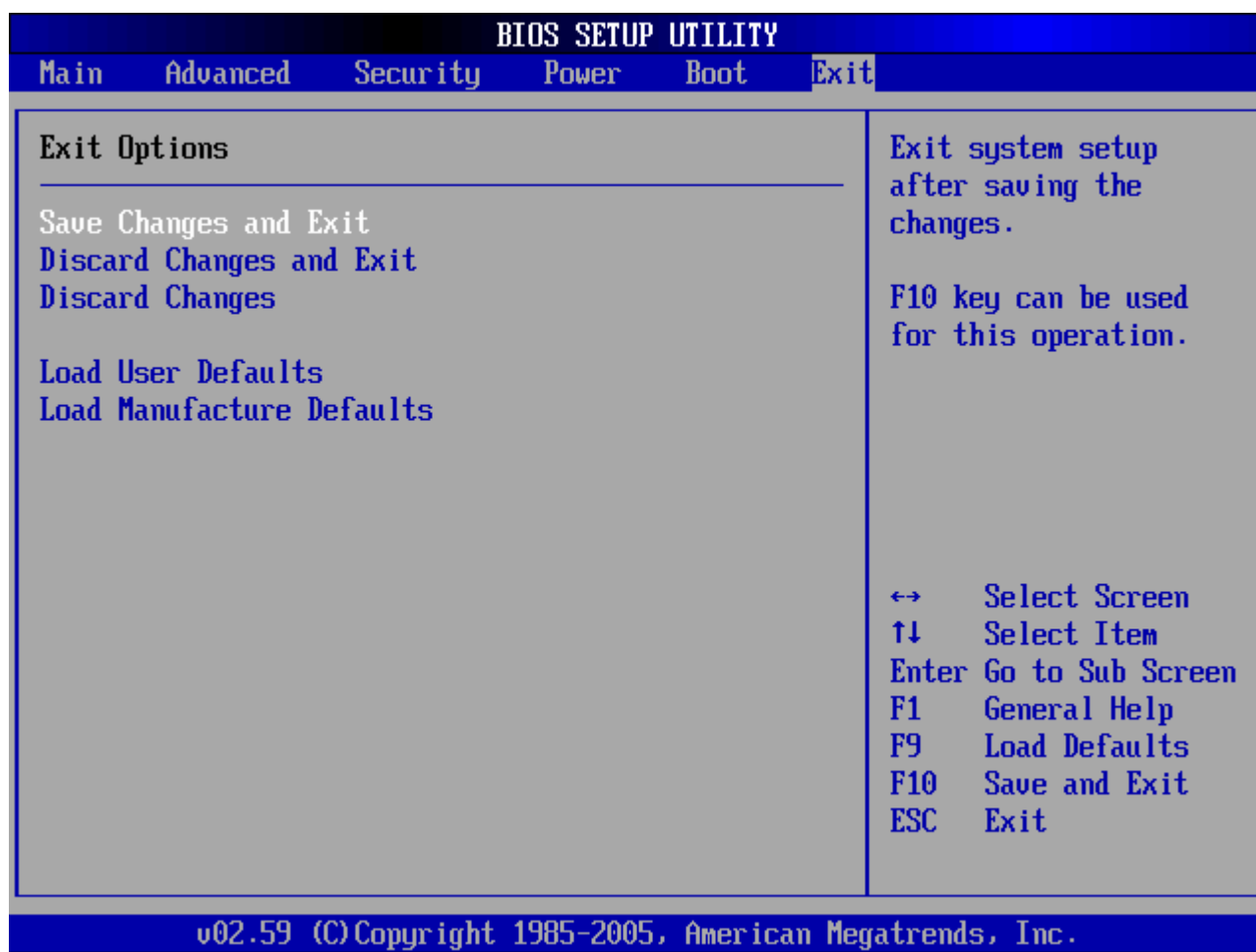
### 3.5. Boot Menu



In this menu users can decide the boot sequence, as long as the device with highest boot priority exists, system BIOS will boot from it, device boot priority is adjusted by pressing “+”, “-” or space key on the selected (highlighted) item. 4 bootable devices for S6FmM system are listed in this menu (BIOS default boot sequence):

1. **Removable device:** ← Legacy floppy.
2. **IDE Hard Drive:** ← hard disk.
3. **ATAPI CD-ROM:** ← CD-ROM
4. **Network Boot:** ← LAN

### 3.6. Exit Menu



Exit BIOS setup, users may make final decision if they want to save the change just made, or load BIOS default setting, lists are:

- Save changes and Exit
- Discard changes and Exit
- Discard Changes
- Load User Defaults
- Load Manufacture Defaults